AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0028] with the following amended paragraph:

[0028] According to another aspect of the present invention, a method of designing a digital filter, the digital filter comprising a tapped delay line made up of a plurality of delay units, the digital filter multiplying the signals of taps by given filter factors and then performing addition and output, characterized in that the method comprises: cascading a basic filter [[~~inn~~]] in n stages (n = 1), the basic filter being constituted using basic filter factors having a symmetrical sequence in which values are set so that the sum is not zero and the sum of every other terms is equal to the sum of the other every other terms with the same signs, and determining, as filter factors for the signals of the taps, nth-order filter factors obtained thus.

Please replace paragraph [0070] with the following amended paragraph:

[0070] FIG. 3 shows frequency-gain characteristics of the results of FFT (Fast Fourier Transfer) performed on the sequences [1] to [4] of FIG. 2. Besides, [[~~again~~]] a gain is standardized at "1" in FIG. 3. As is understood from the characteristic diagram, when the sequence [4] is used as filter factors, a center frequency has a gain of 0. 5 and excellent low-pass filter characteristics can be obtained so that no overshoot occurs in a low frequency area and no ringing occurs in a high frequency area.

Please replace paragraph [0075] with the following amended paragraph:

[0075] FIG. 4 is a diagram showing nth-order filter factors that are obtained by cascading the basic low-pass filter of FIG. 1 [[~~inn~~]] in n stages (n = 1). FIG. 4 shows first-order, second-order, and fourth-order filter factors as representatives. Additionally, the shown filter factors have factor values which are multiplied by 1/32 and is rounded by 10^{-3}.

Please replace paragraph [0093] with the following amended paragraph:

[0093] FIG. 10 is a diagram for explaining transfer which determines filter factors used for the high-pass filter with the fourth-order clock rate 1 from filter factors used for the low-pass

filter with the fourth-order clock rate 1. The following will describe an example where the values of the filter factors are multiplied by 1/32 and are rounded by [[~~i03~~]]10^{-3}. The rounding result of 0 is not shown in FIG. 10.

Please replace paragraph [0110] with the following amended paragraph:

[0110] Subsequently, the number of cascaded stages of the nth-order high-pass filter obtained thus is increased one by one. In this case, since the nth-order high-pass filter is cascaded, a change in cut-off frequency is further reduced following a change of the first-order low-pass filter cascaded [[~~ina~~]] in n stages. Then, the number of cascaded stages is increased until the increasing cut-off frequency exceeds the target cut-off frequency again from the opposite direction (FIG. 18B).

Please replace paragraph [0114] with the following amended paragraph:

[0114] The method for the digital filter and filter design in the present embodiment can be realized any one of a hardware structure, DSP, and software. For example, when the method is realized by software, the digital filter and filter designing apparatus of the present embodiment are actually constituted of the CPU or MPU, [[~~RAN~~]]RAM, ROM, and so forth and are realized by operating programs stored in the RAM and ROM.